

Application Note

System Design Guidelines:

PCB Layout and Circuit Optimization

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1 Introduction

The information of this document is to contain PCB design guidelines and circuit optimization techniques that apply to most designs. These recommendations enable the designer to implement successful, right-first-time, PCB layouts and to ensure trouble free circuit optimization, using the same criteria as those employed by ADChips for the reference designs.

Careful placement and routing with regard to the recommendations described below will ensure that the board will work the first time it is powered up.

2 General Design Information

This document contains design information that applies to the adStar microcontroller including:

- PLL loop filter
- PWM output
- Oscillator
- Power Supply Decoupling Capacitors
- LDO Output Capacitor

2.1 PLL Loop Filter Circuit

The PLL has been realized using an external filter, which allows user to adjust the bandwidth of the PLL, matching a wide range of application requirements. This second order filter should be connected between VCTR and VDD as Figure 2-1.

The Loop filter configurations are illustrated below:

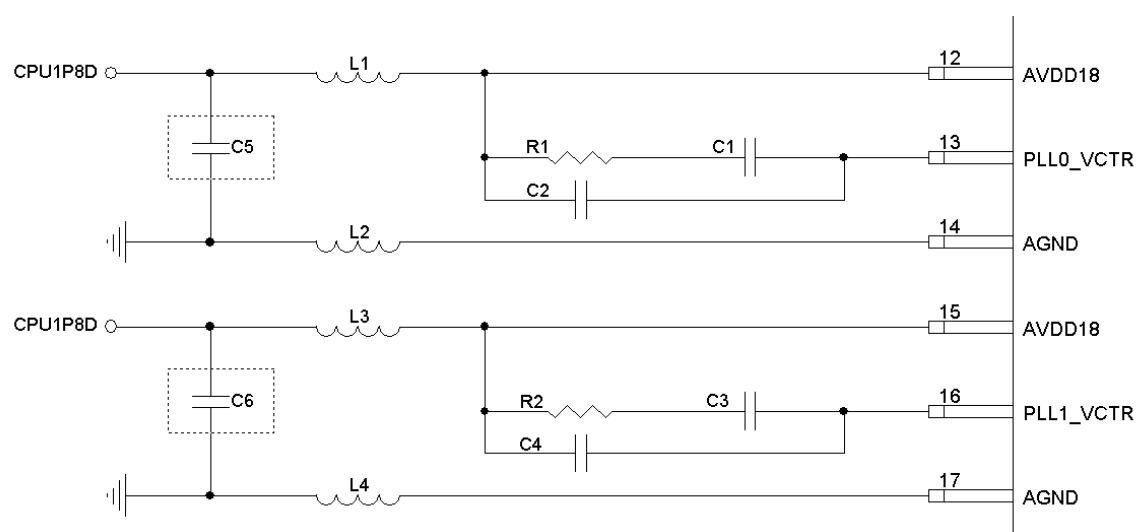


Figure 2-1: External Loop Filter Circuit for PLLs

C5, C6 are optional components (0.1uF ~ 1uF).

Corresponding external filter setting was shown as below:

Table 2-1: LPF Values

XIN * M / N (MHz)	R1/R2 (KΩ)	C1/C3(nf)	C2/C4(pf)
48	2	3.3	220
81	3.3	2	130
120	5	1.3	100
180	7.3	0.9	60
Universal	3.3	2	100

User can set different external LPF values to get optimal performance at different applications,

and a universal external LPF setting can be adopted in all cases to simplify application.

To optimize the PLL Loop filter, it is recommended that the values quoted in Table 2-1 are a good starting point.

2.2 PLL loop filter Layout

The PLL requires a low pass filter. Since this is a sensitive circuit, care should be used to place these components relatively close to the MCU.

The PLL loop filter circuit is illustrated below in Figure 2-2. Again, the PCB trace is kept as short as possible and the loop filter components are partially encased with a guard band. Care should be taken in this area as any noise that is injected into the loop filter will introduce noise in the PLL.

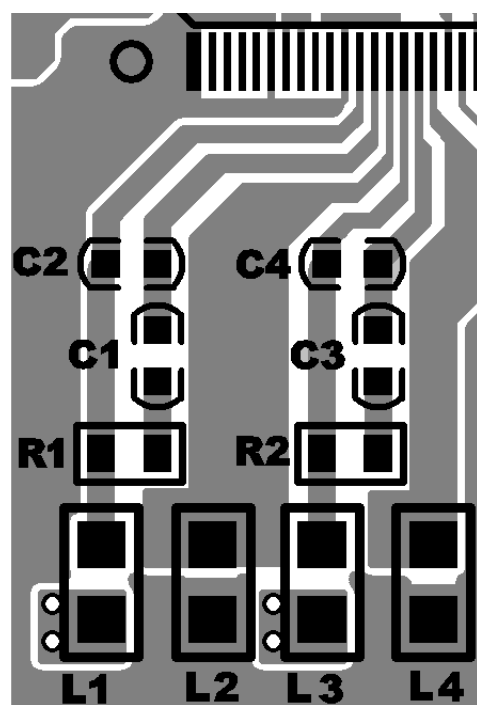


Figure 2-2: Layout Example for PLL Loop Filter

2.3 PWM Output Traces

The oscillator circuitry should be physically isolated or shielded from any I/O signal traces routed to off-board connectors, especially PWM audio I/O signals.

Without these considerations, it results in unreliable or inaccurate operation.

There are some crosstalk issues between oscillator circuit and PWM I/O signals. So follow the below rules:

- Avoid OSC clock and PWM output signal interfering to each other
- PCB layout
 - Protected OSC clock trace by GND separately.

PWM audio I/Os are high-speed and differential signals. Follows the below guide:

- Avoid stubs in A and B in Figure 2-3. Where termination or bias resistors are needed, one terminal should be located directly on the trace like C in Figure 2-3. Both resistors should be located at the same distance from the source and load.

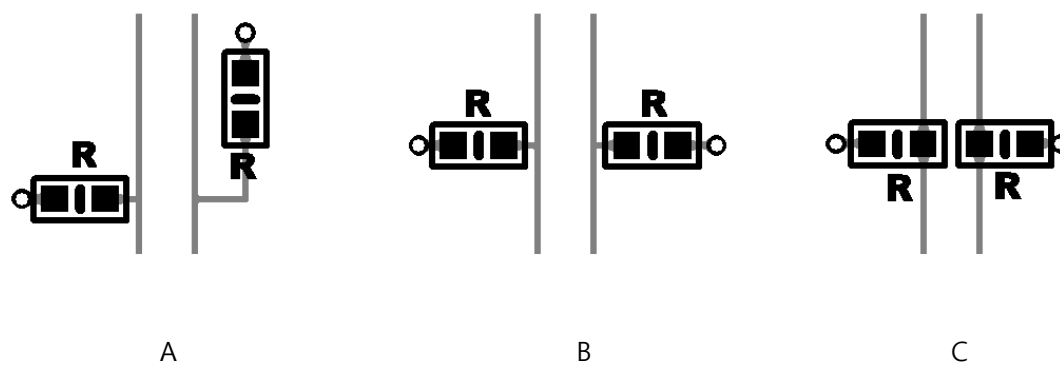


Figure 2-3: Example of Capacitor Placement and Routing

2.4 Oscillator

The oscillator circuit is a primary source to provide a clock for the device.

The on-chip oscillator circuit requires an external crystal and two load capacitors and single resistor to complete the circuit.

To maximize immunity, the oscillator components should be closely grouped and located near to the oscillator pins of the MCU. All traces associated with the oscillator circuit should be as short as possible. The oscillator circuit should be surrounded by guard traces connected to the Vss pin of the MCU with short ground traces or a ground plane. The oscillator circuitry should also be physically isolated or shielded from any I/O signal traces routed to off-board connectors. Layouts that incorporate these rules are shown in Figure 2-4. Ideal trace length is less than 0.25"/6mm. Do not exceed 0.5"/12mm.

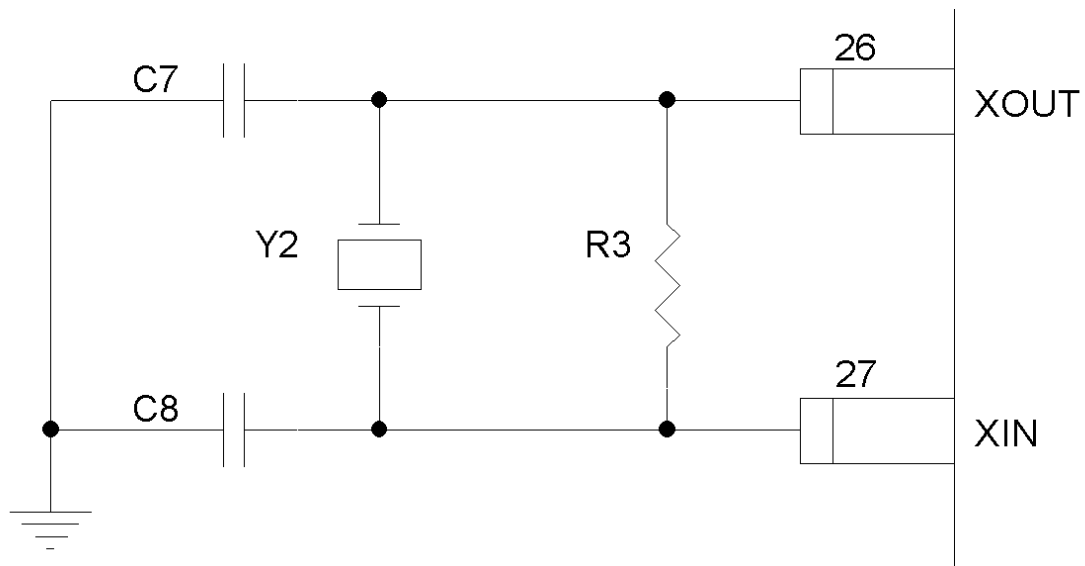


Figure 2-4: Recommend Circuit for Crystal

Table 2-2: Component Value

Product	C7	C8	R3	Y2
Value	18pF	18pF	150K	10MHz

The layout in Figure 2-5 is possible layout example which correctly applies the filtering and crystal layout guidelines.

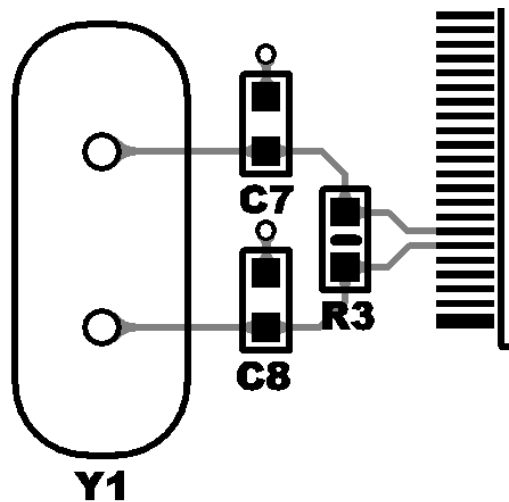


Figure 2-5: Layout Example for Crystal

2.5 Power Supply Decoupling Capacitors

Power supply decoupling is very important for optimal operation of the adStar. To keep the loops are small, place these capacitors right next to the IC. Use the shortest possible traces to the IC. Ideally, the traces on each side of the capacitor should be the same length and run in the same direction to avoid differential noise during ESD. If possible, place a via near the VSSD pin to the digital ground plane and another from near the VSSA pin to the analog ground plane.

Figure 2-6 is an example of what to do.

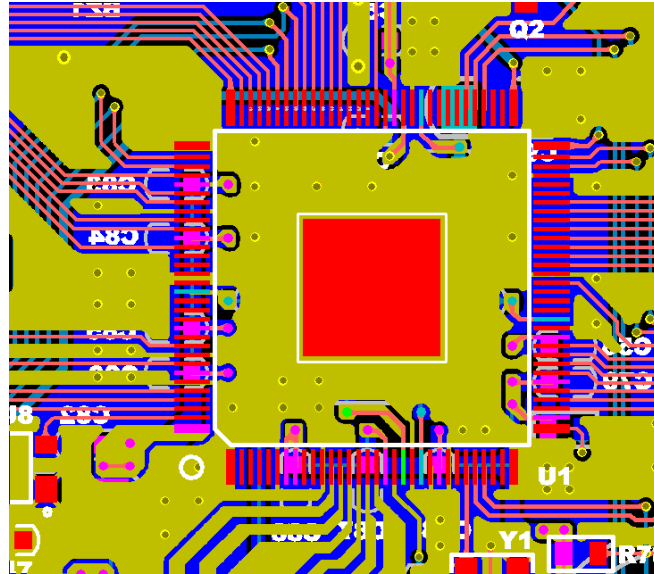


Figure 2-6: Example of Decoupling Capacitor Placement and Routing(TOP)

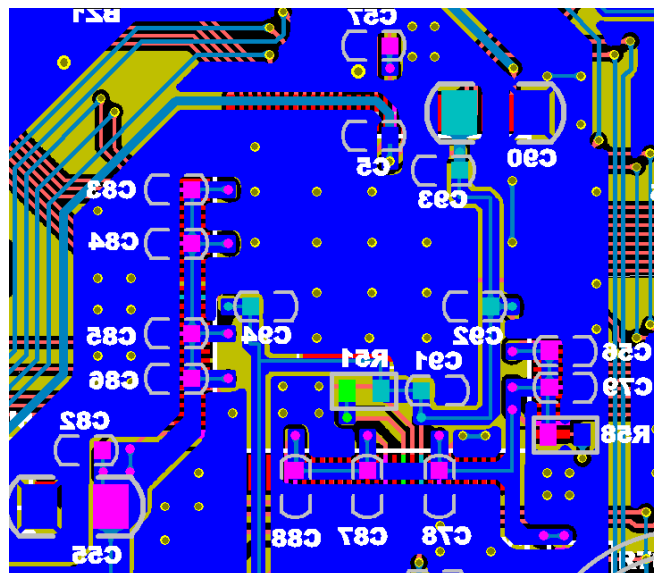


Figure 2-7: Example of Decoupling Capacitor Placement and Routing(BOTTOM)

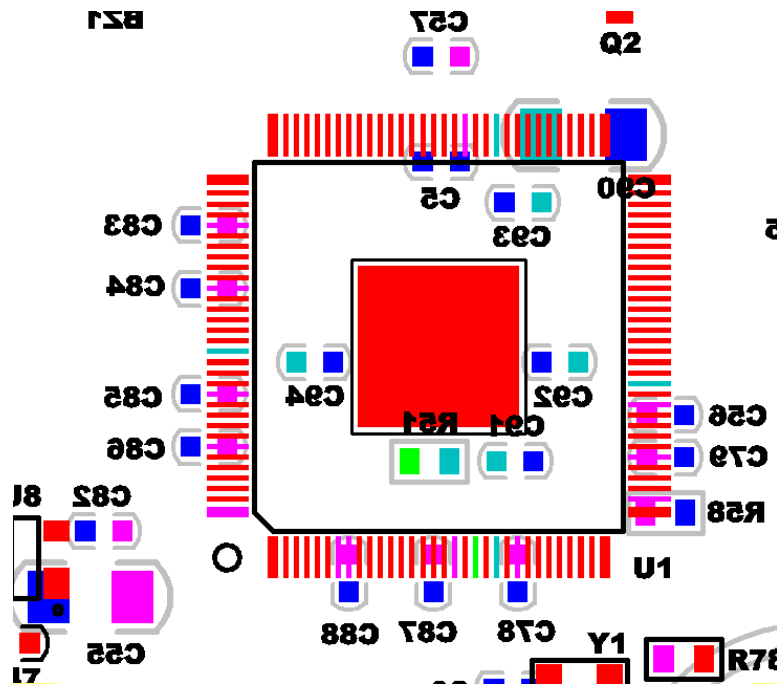


Figure 2-8: Example of Decoupling Capacitor Placement and Routing(SILK)

2.6 LDO Output Capacitor

The adStar has on-chip LDO regulator that +1.8V power supply(VDDC) is generated internally. So only a single +3.3V power supply required.

The device also allows VDDC to be provided from an external regulator, see the adStar's data sheet.

Even if an external regulator is used for VDDC source, the on-chip LDO regulator must still have a capacitor on its output. See Figure 2-9 for details.

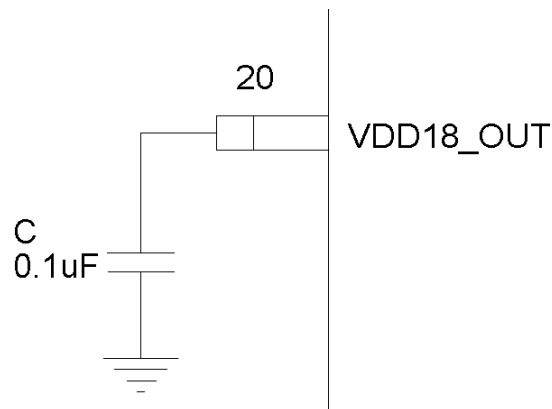


Figure 2-9: Example Circuit when On-chip LDO not Used