adStar-L
High-Performance 32-bit Microcontroller
with 8-/16-MB SDRAM

Description

adStar-L is designed to provide a cost effective, low power and high performance microcontroller solution as LCD display applications and general applications. adStar-L integrated microprocessor combines a 32-bit advanced EISC processor core and SDRAM with several peripheral functions such as JPEG decoder, RTC, USB, flash memory controller, etc. The on-chip cache and SRAM provide one-cycle access to code and data to speed program execution.

Features

High Performance Processor Core
- 32-bit EISC CPU Core
- Harvard Architecture
- 5-Stage Pipelining
- 1-Cycle 32-bit MAC
- 8KBytes I-Cache, 8KBytes D-Cache
- Up to 120MIPS throughput with 120MHz Clock

Additional Embedded Memory
- 3KBytes SRAM (1KBytes Data/2KBytes Instruction)
- 8-/16-MBytes SDRAM

Boot Mode
- Flash Booting Mode
- External Nand Flash Booting Mode

LCD Interface
- SPI 9Bit Interface
- RGB 888/565 Interface

USB Full-Speed Host/Device Compatible
- Supports Full-speed Data Rate 12Mbps

JPEG Decoder
- Supports JPEG decoding by hardware

RTC
- Time: Hours, Minutes and Seconds
- Alarm Interrupt supported

Debug Interface
- SWD(Serial-Wire Debug) supported

Software Library
- MP3 Software Decoding

Sound Mixer
- 4-ch. Mixing
- 1-ch PWM output for Stereo or 2-ch PWM output for Mono

Clock, reset, Power management
- 32KHz osc I/O for RTC external crystal
- Internal 2 PLL output clock
- POR reset
- Several Power Modes supported

Other Peripheral Functions
- 4-ch. 32-bit Timer/PWM/Capture
- 32-bit Core Timer (for Tick)
- DMA Controller
- SD Card Controller
- Nand Flash Controller (4-,24-bit ECC)
- 32-bit Watchdog Timer
- Interrupt Controller
- 2-ch. UART
- Master/Slave SPI
- TWI (Two Wired Interface)
- 55 Port I/Os (muxed with other interfaces)

Analog Functions
- POR (Power On Reset)
- LDO
- PLL0(for system), PLL1(for LCD)
- 1-KSPS 4-ch. Input 12-bit ADC

Operating Voltage : 3.0V to 3.6V
Package : 100 Pin TQFP

Product Matrix

Product Code	SDRAM	FLASH
adStar-L8M	8MB	-
adStar-L8MF512	8MB	512KB
adStar-L16M	16MB	-
adStar-L16MF512	16MB	512KB

Application

- LCD Display Applications
- Smart Home Appliance(Refrigerator, Washing Machine, Air Conditioner, Rice Cooker, etc)
- POS System - Sign-Pad - POP Monitor - Industrial Controller - Access Controller

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Instruction Highlights

What is EISC ISA?
Adchips' patented EISC (Extendable instruction Set Computer) ISA is a compress RISC typed instruction set that can reduce the program size and the frequency of the memory access efficiently for optimizing energy consumption.

AE32000C ISA
AE32000 stands for 32-bit advanced EISC ISA family. In the revision C, various SIMD-typed DSP instructions are added for accelerating DSP instructions are added for accelerating DSP applications.

32bit Data Processing
AE32000C processors have 32-bit data processing units such as 32-bit ALU, barrel shifter, multiplier and MAC (multiply and accumulator) and so on.

4G Memory Space
AE32000C processors can access up to 4G memory space.

Various Cond. Branches
14 type conditional branches bring more compactor control sequences and less energy consumption.

Multiple PUSH/POP
AE32000C processor support multiple PUSH and POP instruction for efficient context switching.

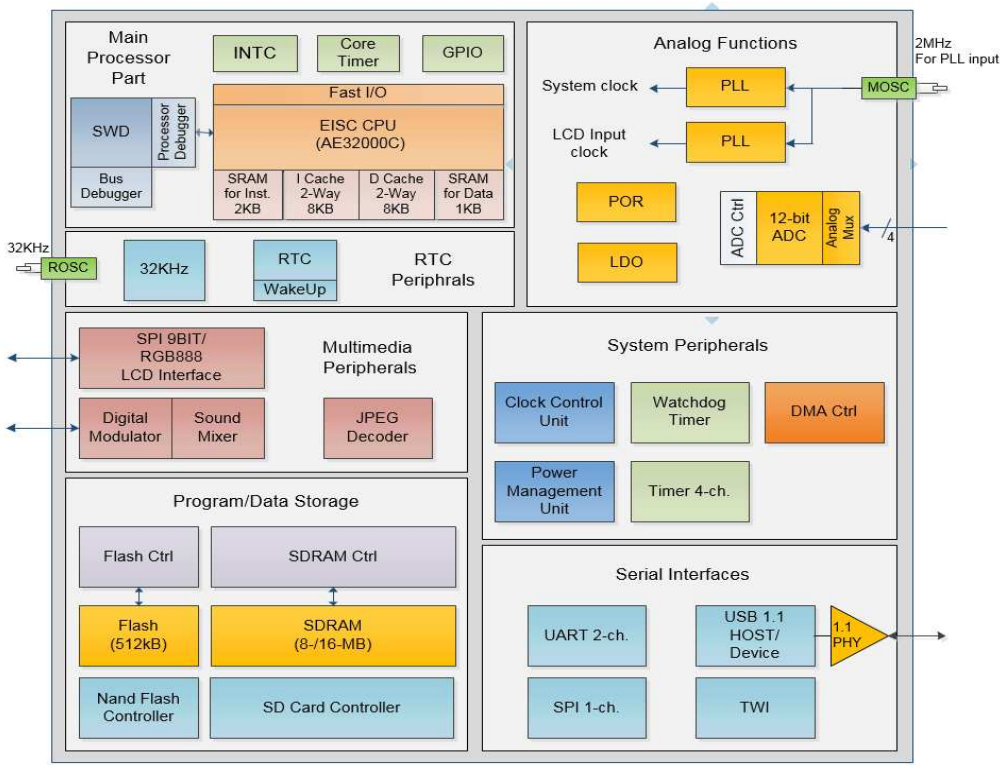
3 Processing Mode
AE32000C supports supervisor mode, user mode and hypervisor mode for advanced resource protection.

SIMD-DSP Extension
AE32000C supports SIMD-DSP instructions such as 32-bit MAC with 80-bit accumulator, 8-bit and 16-bit SIMD MAC, sum-of-products operation, saturated add/subtract, min/max, average and so on.

Rich Registers
16 x 32-bit GPRs
9 x 32-bit SPRs
3 Stack Pointers

Why EISC?
EISC offers energy efficiency for Your SoC in any applications

Block Diagram



Comparison adStar-L vs. adStar-D

Functions	adStar-L	adStar-D
Max. Operation Frequency	120Mhz	108Mhz
UART	2-ch	4-ch
SPI	1-ch	2-ch
I²S	-	2-ch
Timer	2-ch	5-ch
DMA	6-ch	8-ch
Sound Output	Stereo 1-ch	Stereo 2-ch
Max. GPIO	55	75
LCD Interface	Serial & Parallel	Parallel
A/D Converter	12bit	10bit
JPEG Decoder	H/W	S/W
RTC	O	-
Low Power Management	O	-
Copy Protection	-	O
Debug Interface	SWD	JTAG
Package Type	100 Pin TQFP	128 Pin ETQFP

EISC Studio Software
EISC-Studio is an integrated development environment tool for the developers who are using EISC CPU in Windows environment. EISC-Studio provides convenient source editor, compile and debug tools while user implements a system and also, various images of high level programming language and executable code for source level debugging.

EISC
www.adc.co.kr