Amazon-II

High-Performance HD Graphics Microcontroller

adc
advanced digital chips inc.

Description

AMAZON-II is a HD graphics microcontroller. AMAZON-II is a super integrated SoC (system on a chip) aimed at providing high performance graphics functionality and low power consumption.

AMAZON-II incorporated 32-bit CPU processor with 2D graphics engine, DDR2 controller, JPEG decoder ,sound mixer, display controller with OSD, video encoder, video decoder interface module, USB host/device and other I/O peripheral components. AMAZON-II can reduce system cost significantly through eliminating not only system control CPU, but also graphics IC, sound IC and video encoder as well as USB.

AMAZON-II helps system designers to reduce its engineering effort and time in developing a new system by adding only memory and I/O devices such as LCD panel, flash and etc.

Features

High Performance Processor Core
- 32-bit EISC CPU core
- 16-bit fixed length instruction set
- Harvard architecture
- 9-stage pipelining
- 8KBytes I-cache, 8KBytes D-cache
- Up to 200MIPS throughput with 200Mhz clock

2D Graphics Engine
- Supports 16/8/4-bit color mode
- Supports 24-bit with alpha color mode
- Supports tile addressing / font addressing mode
- Supports texture mapping(zoom in/out, rotate, iteration, clipping)
- Supports shading, alpha blending, transparency and dithering(2x2, 4x4)

JPEG Decoder
- ISO 10918-2 base line JPEG decoder
- Only supports typical huffman table defined in annex K of standard
- Supports YCbCr 4:2:2 / 4:2:0 format
- Supports up to 2048x2048 pixel image

Sound Mixer
- Audio mixing and recording
- Supports 2-ch. PCM wave playback and 1-ch. record
- Re-sampler
- Supports 8kHz~96kHz sampling rates
- 32-depth buffer per each channel
- 8-bit and 16-bit input data format
- Integrated I^2S master interface output

Video Interface
- Supports BT.656 input format
- Output formats
  - Component RGB video for VGA
  - CVBS analog output for TV(NTSC/PAL)
  - YPbPr output for HD output
  - Digital RGB 888 for LCD
- Support on-screen display(OSD)
- Support HD resolution (up to1280 x 720)

SDRAM Interface
- 16-bit data width
- Supports for DDR2 and mobile DDR

SRAM/ROM/NOR Interface
- 8/16-bit data, up to 22-bit addressing

Serial Flash Interface
- Supports Single/Double/Quad bit data transfer

NAND Flash Interface
- Supports SLC and MLC (4/24-bit ECC) type

SD-Card Interface
- Supports single/quad bit data transfer

USB Host / Device Interface
- Supports full-speed data rate 12Mbps

JTAG Interface
- Boundary-scan capabilities
- Supports extensive on-chip debug
- Programming of flash through the JTAG interface

Other Peripheral Functions
- 4-ch. 16-bit timer/counter with 15-bit pre-scaler, capture and PWM
- 32-bit watchdog timer
- Interrupt controller
- 4-ch. UART (with 1-ch. supports IrDA)
- 2-ch. SPI master/slave
- TWI (Two Wired Interface)
- 4-ch. AHB DMA, 2-ch. AXI DMA
- I^2S interface
- 116 port I/O (muxed with other interface ports)

Operating Voltage
- I/O 3.3V, DDR2 I/O 1.8V, Core 1.2V

Package
- 289 FBGA 15x15 (0.8 ball pitch)

Application Areas

Video/Graphics
- Video Door Phone, Digital Picture Frame,
- Access Control System, Arcade Game Machine

Medical
- Patient Monitoring System, Medical Meters

Automotive
- Infotainment System, Digital Instrument Cluster
- Automotive HMI (Trip Computer)

Industrial
- HMI(Human Machine Interface), LCD Module(LCM)

Advanced Digital Chips, Inc. http://www.adc.co.kr

Korea (Headquarters)
22F, Bldg A, Keumkang Penterium IT Tower,
810 Gwanyang-dong, Dongan-gu, Anyang-si,
Gyeonggi-do, 431-060, Korea
T : +82-31-463-7500 / F : +82-31-463-7588
E-mail : eisc@adc.co.kr

China
Peak Microtech Co., Ltd
北京芯首电子科技有限公司
E-mail : sales@peaktech.com.cn
http://www.peaktech.com.cn

EISC
New Embedded Microprocessor

Instruction Highlights

What is EISC ISA?
Adchips' patented EISC (Extendable instruction Set Computer) ISA is a compress RISC typed instruction set that can reduce the program size and the frequency of the memory access efficiently for optimizing energy consumption.

AE32000C ISA
AE32000 stands for 32-bit advanced EISC ISA family. In the revision C, various SIMD-typed DSP instructions are added for accelerating DSP instructions are added for accelerating DSP applications.

32bit Data Processing
AE32000C processors have 32-bit data processing units such as 32-bit ALU, barrel shifter, multiplier and MAC (multiply and accumulator) and so on.

4GB Memory Space
AE32000C processors can access up to 4G-byte memory space.

Various Cond. Branches
14 type conditional branches bring more compactor control sequences and less energy consumption.

Multiple PUSH/POP
AE32000C processor support multiple PUSH and POP instruction for efficient context switching.

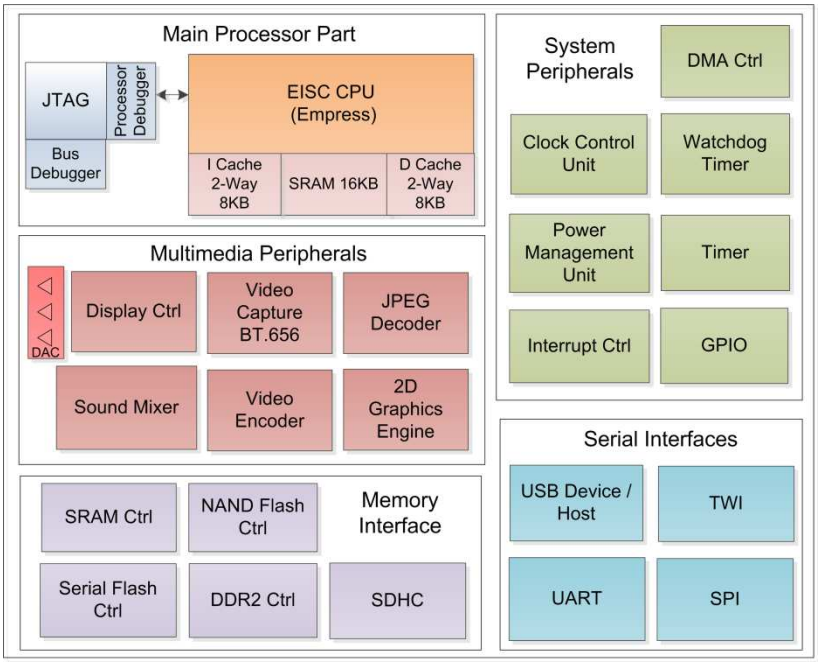
3 Processing Mode
AE32000C supports supervisor mode, user mode and hypervisor mode for advanced resource protection.

SIMD-DSP Extension
AE32000C supports SIMD-DSP instructions such as 32-bit MAC with 80-bit accumulator, 8-bit and 16-bit SIMD MAC, sum-of-products operation, saturated add/subtract, min/max, average and so on.

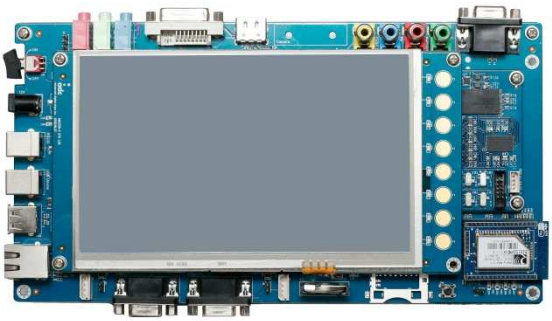
Rich Registers
16 x 32-bit GPRs
9 x 32-bit SPRs
3 Stack Pointers

Why EISC?
EISC offers energy efficiency for Your SoC in any applications

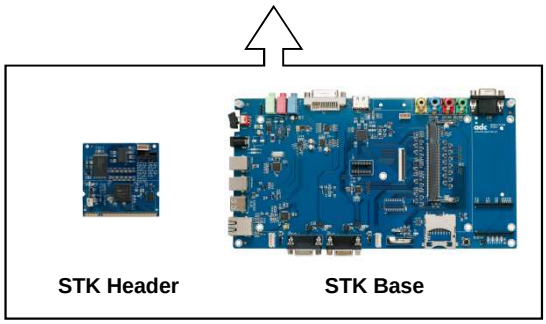
Block Diagram



Development Board



AMAZON-II STK SET



Features

AMAZON-II STK Header
- CPU : AMAZON-II
- DDR2 : 1Gbit
- Nand Flash : 4Gbit
- Serial Flash : 64Mbit
- 1ch. UART
- JTAG Debugging Port
- Power 5V

AMAZON-II STK Base
- HDMI / DVI / VGA Out
- CVBS In/Out
- YPbPr Out
- USB Host/Device
- SD Card Socket
- CAN Port
- RJ-45 for Ethernet
- Audio In/Out
- Real Time Clock
- Wi-Fi (option)
- Power 12V

LCD Module
- 7" TFT-LCD(1024X600) with touch panel
- 8-ch. capacitive touch sensor

EISC Studio Software Tool

EISC-Studio is an integrated development environment tool for the developers who are using EISC CPU in Windows environment. EISC-Studio provides convenient source editor, compile and debug tools while user implements a system and also, various images of high level programming language and executable code for source level debugging.