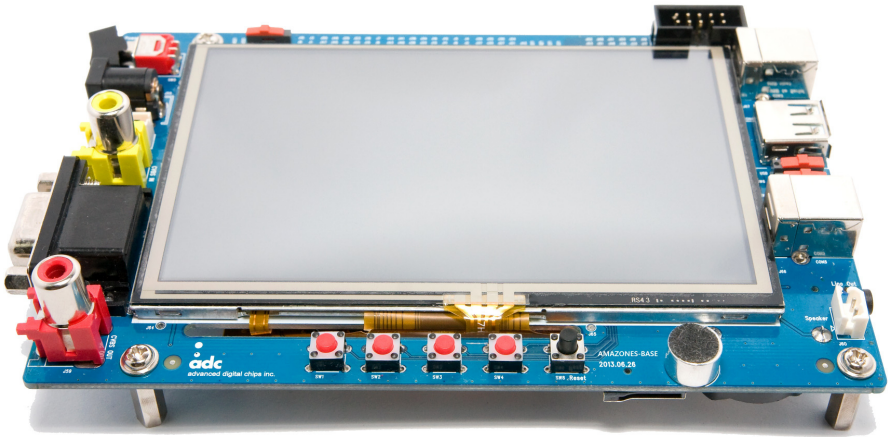
adc
advanced digital chips inc

User's Manual

AMAZONES-BASE



Ver 1.2

MAR. 30, 2017

Revision history

Date	Doc. Rev		Changes
26-AUG-14	Rev. 1.0		Initial Release
02-MAR-17	Rev. 1.1		표 2-1. 표 2-2
30-MAR-17	Rev.1.2		EIRQ1 Remove

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1. Introduction

AMAZONES-BASE는 AMAZONES를 사용하는 user를 위한 예제 보드이다. AMAZONES에 LCD, TOUCH, UART, USB, sd card등을 설계하여 AMAZONES의 기본 동작에 충실한 예제를 제공한다.

2. AMAZONES-BASE

2-1 Feature

AMAZONES Socket

- 0.5mm 100Pin Socket x 2

Serial Flash

- 64Mbit 80MHz SPI Multi I/O

LCD

- HD50WVPF1
- Interface: RGB 888
- Resolution: 800x480
- LED Backlight: V_f(19.2V), I_f(40mA)
- Touch: 4wire resistive type

External Video Input

- CVBS Input(720x480 Only)

Analog Video Output

- VGA Output
- CVBS Output

Audio

- Mono CODEC
- 40mW/16Ohm/3.3V

RTC

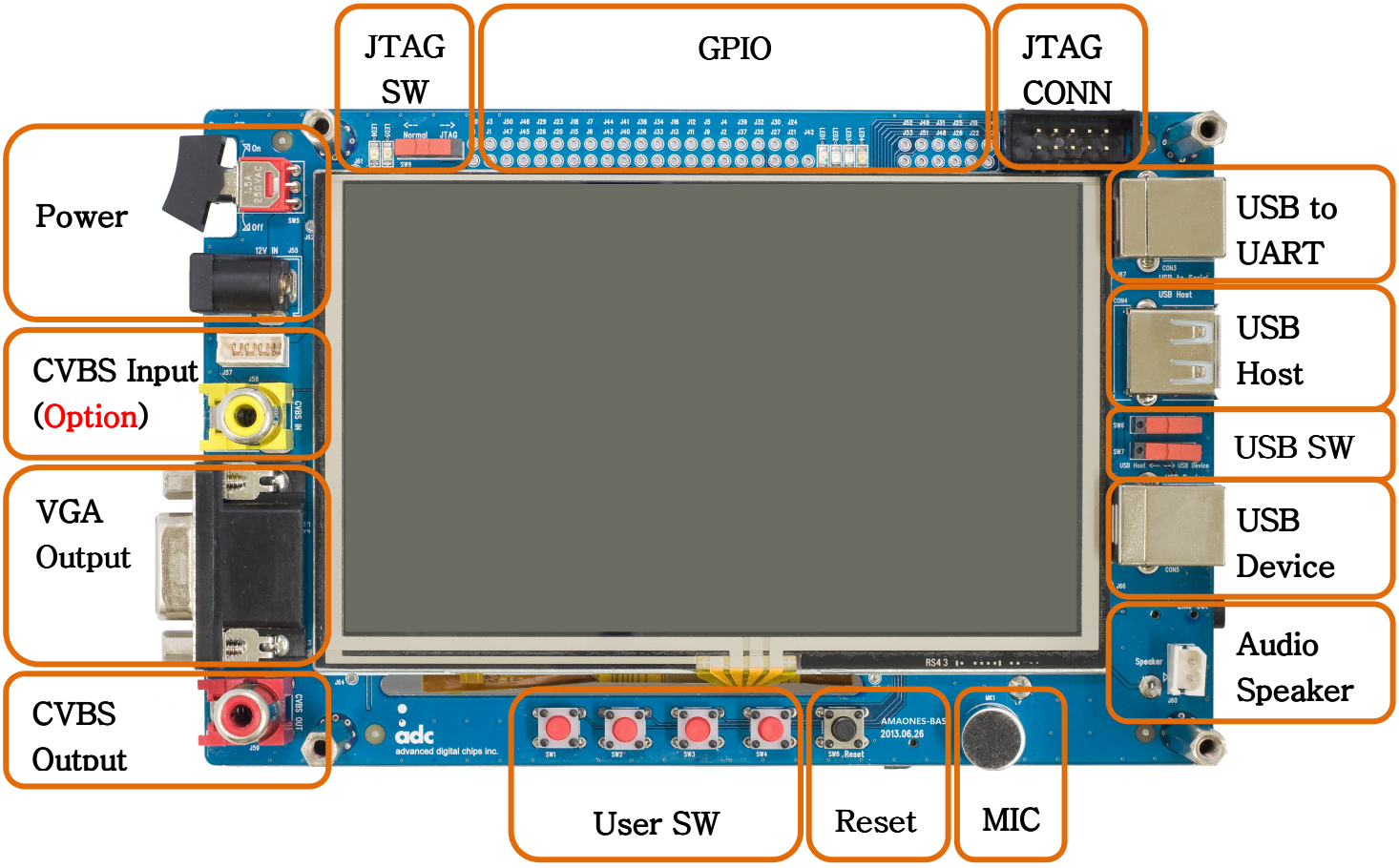
UART

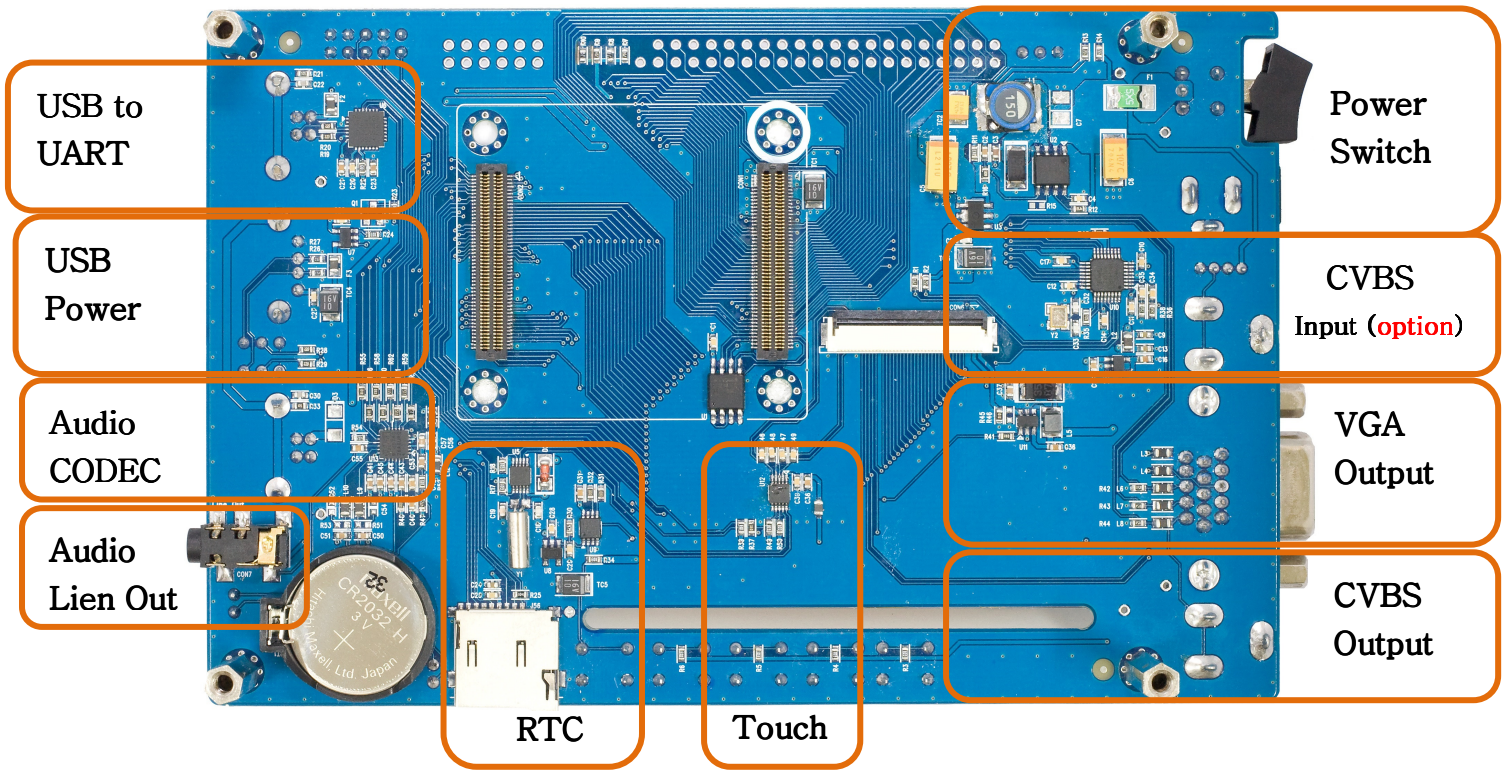
- USB to Uart

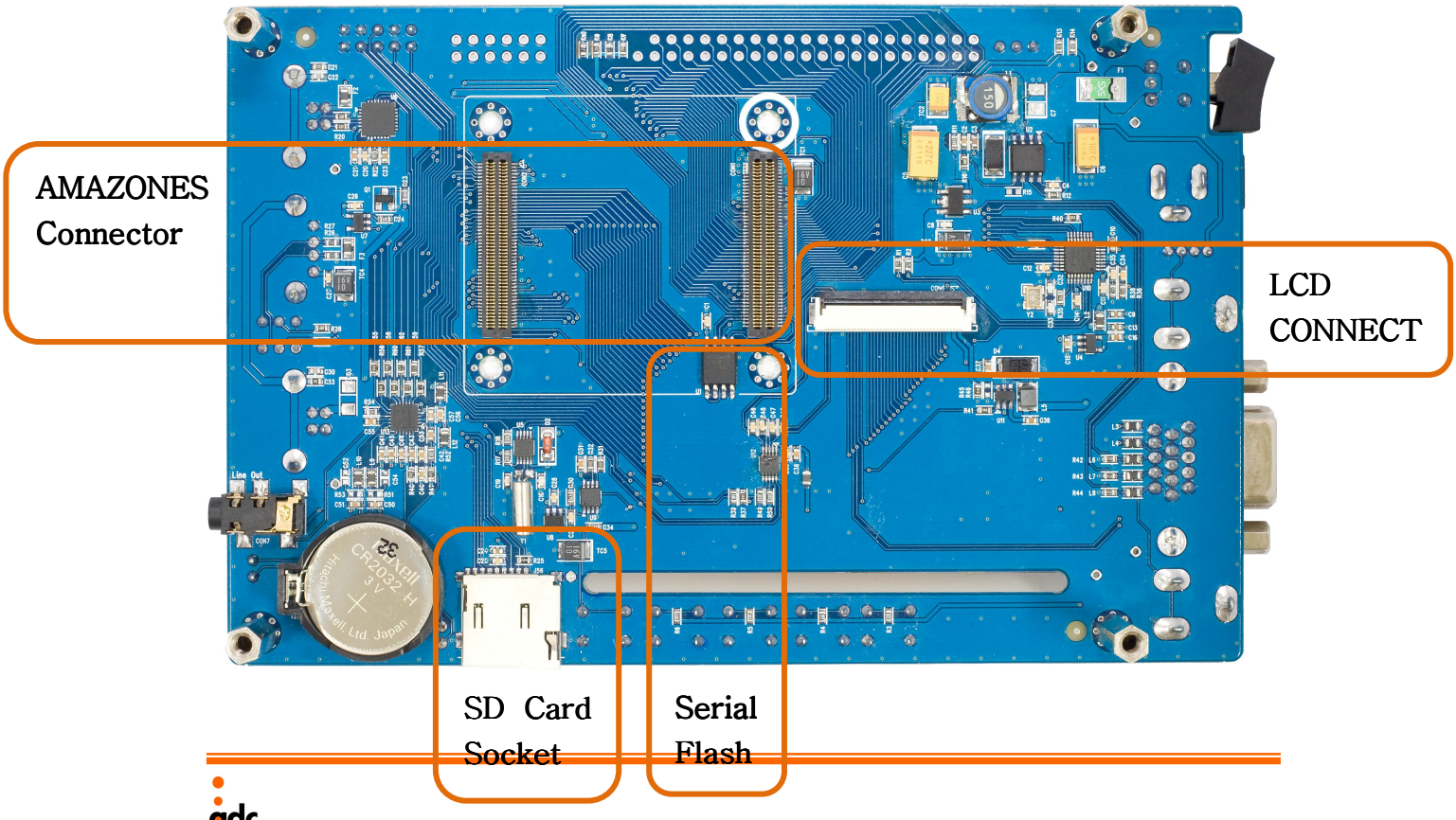
Power

- 12V/1A Power Input

2-2 AMAZONES-BASE board 구성



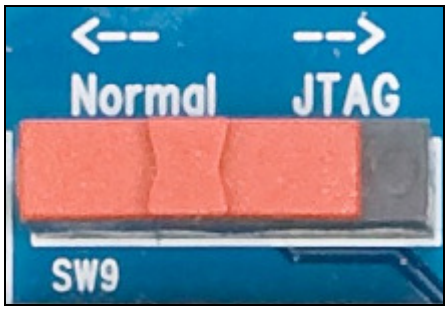

USB to
UART
USB
Power
Audio
CODEC
Audio
Lien Out
RTC
Touch
Power
Switch
CVBS
Input (option)
VGA
Output
CVBS
Output


AMAZONES
Connector
SD Card
Socket
Serial
Flash
LCD
CONNECT

2-3 JTAG Mode Select(SW9)

AMAZON-II의 JTAG mode를 설정하는 Switch이다.

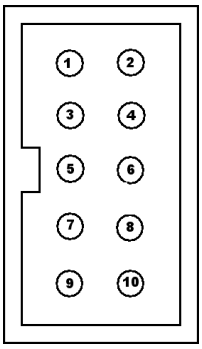
JTAG mode는 switch를 오른쪽(Low)으로 이동하면 JTAG mode가 되고 왼쪽으로 이동하면 Normal boot mode가 된다.



2-4 JTAG Connector(J54)

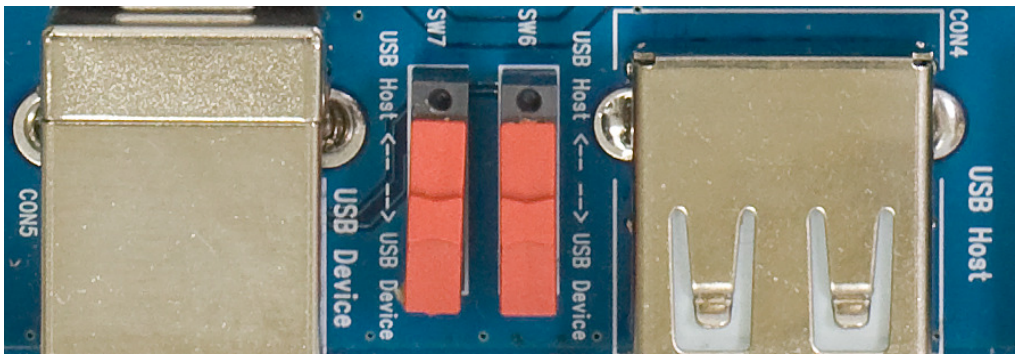
AMAZONES의 AMAZON-II을 debugging하거나 NAND Flash에 data를 download하기 위한 connector이다.

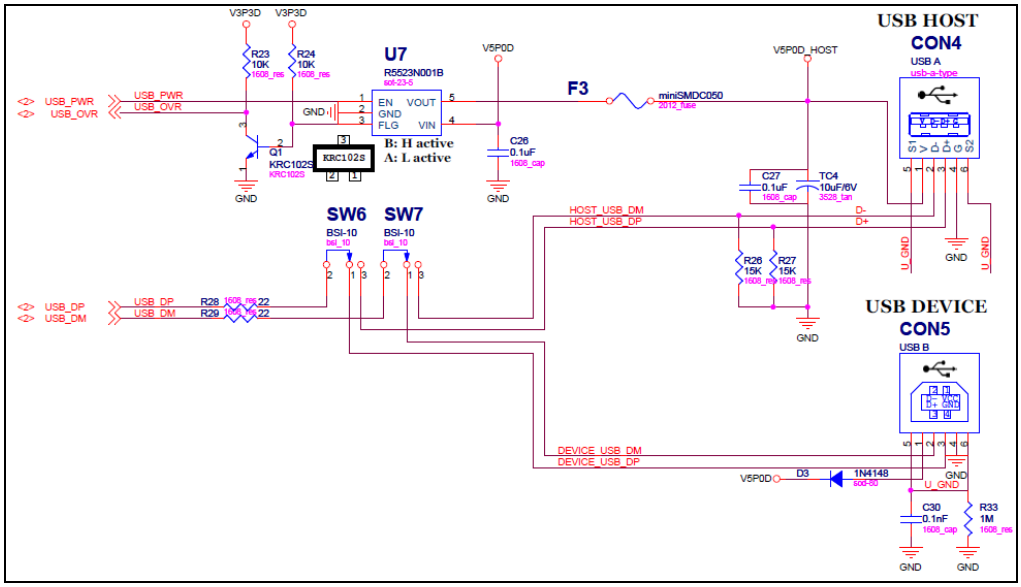
JTAG Connector(J54)			
Pin NUM	**Pin Name**	**Pin NUM**	**Pin Name**
1	TDI	2	NC
3	TMS	4	GND
5	TRST	6	TDO
7	TCK	9	GND
9	GND	10	GND



2-5 USB(CON4, CON5, SW6, SW7)

USB Host/Device를 지원한다. USB Host/Device 선택은 SW6, SW7로 설정한다.





Host Power는 U7 R5523N001B를 control하여 On/Off한다.

2-6 UART(CON3)

AMAZONES-BASE는 UART to USB를 사용하여 debugging message를 출력 할 수 있다. UART channel은 0번을 사용한다.

2-7 Audio CODEC

Audio CODEC은 WM8974CGEFL으로 mono이며, Input은 Microphone을 사용하고 출력은 Line out/Speaker out을 사용한다. Speaker out은 3.3V에서 8Ω에서 0.9W을 출력 할 수 있다.

→Microphone

Microphone(MK1)	
Pin NUM	**Pin Name**
1	Microphone negative
2	Microphone positive

→Line Out

Line Out(CON7)	
Pin NUM	**Pin Name**
1	GND
2	Line Out
3	NC
4	NC
5	NC

→Speaker Out

Speaker Out(J60)	
Pin NUM	**Pin Name**
1	Speaker negative
2	Speaker positive

2-8 User Switch

사용자를 위한 switch는 4개로 GPIO에 할당 되어있다.

User Switch(SW1, SW2, SW3, SW4)	
Switch NUM	**GPIO NUM**
SW1	GPIO14.7
SW2	GPIO14.6
SW3	GPIO14.5
SW4	GPIO10.4

2-9 Display

AMAZONES-BASE는 LCD, VGA, CVBS의 3가지를 display 할 수 있다.

→LCD

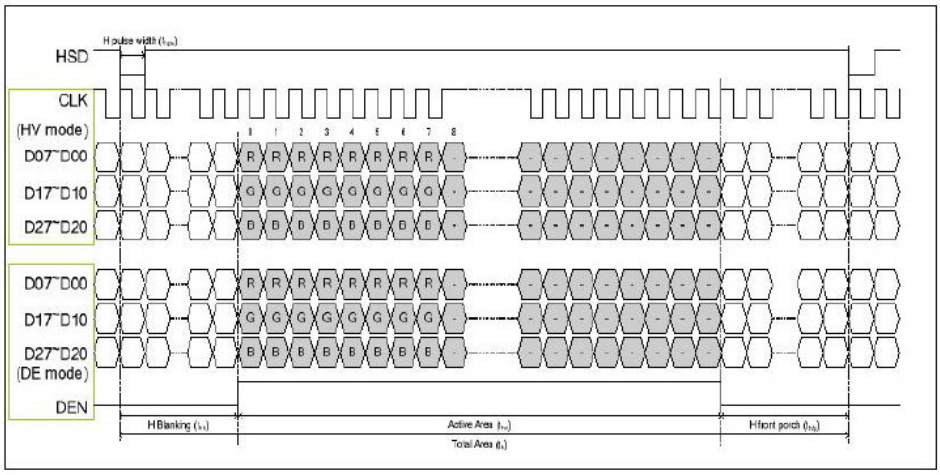
LCD는 HD50WV-PF1으로 5"+touch(4wire resistive)가 포함된 LCD이다.

LCD Connector*CON6)			
Pin NUM	**Pin Name**	**Pin NUM**	**Pin Name**
1	LED Cathode	21	BLUE0
2	LED Anode	22	BLUE1
3	GND	23	BLUE2
4	VCC(3.3V)	24	BLUE3
5	RED0	25	BLUE4
6	RED1	26	BLUE5
7	RED2	27	BLUE6
8	RED3	28	BLUE7
9	RED4	29	GND
10	RED5	30	PCLK
11	RED6	31	LCD ON/OFF
12	RED7	32	HSYNC
13	GREEN0	33	VSYNC
14	GREEN1	34	Display Enable
15	GREEN2	35	NC
16	GREEN3	36	GND
17	GREEN4	37	XR
18	GREEN5	38	YD
19	GREEN6	39	XL
20	GREEN7	40	YU

-LCD Control Register 설정 방법

(1) Horizontal timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
Horizontal display area	thd		800		DCLK
DCLK frequency	fclk	-	30	50	MHz
One horizontal line	th	889	928	1143	DCLK
HS pulse width	thpw	1	48	255	DCLK
HS back porch (Blanking)	thb		88		DCLK
HS front porch	thfp	1	40	255	DCLK
DE mode blanking	th-thd	85	128	512	DCLK



[Horizontal input timing diagram]

위의 그림은 HD50WV-PF1의 Horizontal timing이다.

LCD Dot Clock frequency는 30MHz로 Horizontal frequency는 30MHz/928=32KHz이다.

Vertical frequency= 32KHz/525=60Hz

HT(Horizontal Total)=th(One Horizontal line)

HSS(Horizontal Sync Start)=thfp(HS front porch)

HSE(Horizontal Sync End)=HSS+thpw(HS pulse Width)

HAS(Horizontal Sync Active Start)=HSS+thb(HS back porch)

HAE(Horizontal Sync Active End)=HAS+thd(HS display area)

HT=928

HSS=40

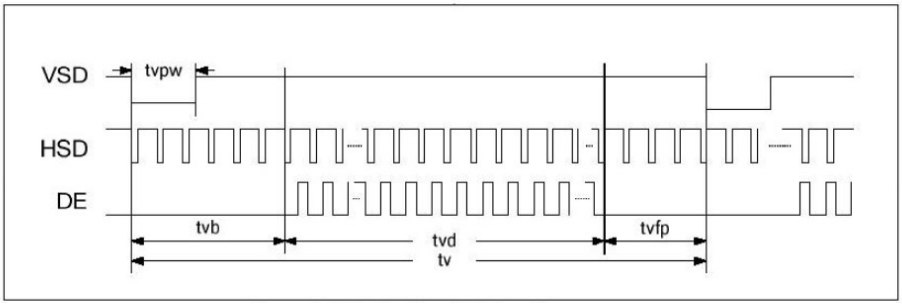
HSE=40+48=88

HAS=40+88=128

HAE=40+88+800=928

(2) Vertical timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
Vertical display area	tvd		480		T_H
VS period time	tv	513	525	767	T_H
VS pulse width	tvpw	3	3	255	T_H
VS back porch (Blanking)	tvb		32		T_H
VS front porch	tvfp	1	13	255	T_H
DE mode blanking	tv-tvd	4	45	255	T_H



[Vertical input timing diagram]

VT(Vertical Total)=tv(One Vertical line)

VSS(Vertical Sync Start)=tvfp(VS front porch)

VSE(Vertical Sync End)=VSS+tvpw(VS pulse Width)

VAS(Vertical Sync Active Start)=VSS+tvb(VS back porch)

VAE(Vertical Sync Active End)=VAS+tvd(VS display area)

VT=525

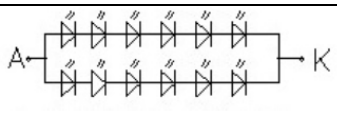
VSS=13

VSE=13+3=16

VAS=13+32=45

VAE=13+32+480=525

→LED Backlight



[Backlight circuit diagram]

(Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Condition	Note
Supply vol.	Vf	-	19.2	-	V	If=20mA, Vf=3.2/LED	-
Supply current.	If	-	40	-	mA		
Luminance (1)	L	400	500	-	Cd/m^2		
Luminance Uniformity	U_L	75	80	-	%		
Life time (2)	-	20000	-	-	Hr		
Color of LED	White						

Backlight는 LED로 순방향 전압이 19.2V로 공급 전류는 40mA로 설계 되어야 한다.

따라서 공급 전압은 19V, 전류는 V_{fb}=1.0V , R46=22Ω이므로 1.0V/22=45mA로 설계 되었다.

Touch는 4wire resistive로 AK4183을 사용하고 눌러지면 EIRQ1으로 Interrupt가 발생되며 이때 TWI로 좌표 값을 읽으면 된다.

→Analog (VGA: P1, CVBS: J59)

Analog RGB의 최대 해상도는 1024x720이다.

CVBS 출력은 Red pin에 MUX되어 있다.

DAC voltage level은 White일 경우 MAX 1V이다.

DAC 출력 전압 조절은 V_{ref} 및 R_{set}, R_{out}으로 조절 한다.

R_{out}=75Ω

R_{set}=2KΩ

V_{ref}=1.235V

$I_{out}=(V_{ref}*1023)/(32*R_{set})$

$I_{out}=(1.235V*1023)/(32*2K\Omega)$

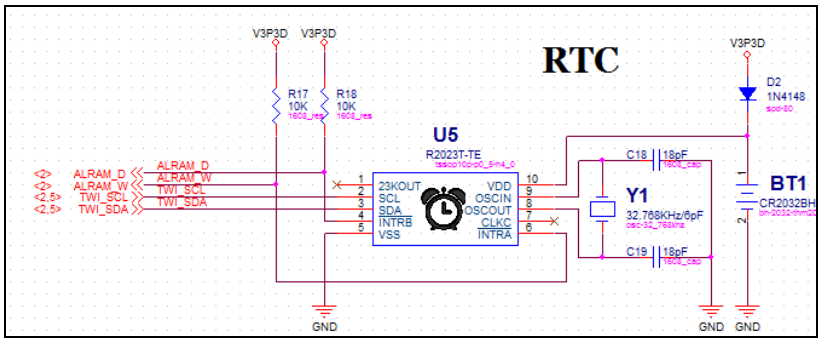
I_{out}=19.7mA

$V_{out}=I_{out}*R_{out}$

V_{out}=19.7mA*75/2=0.74V

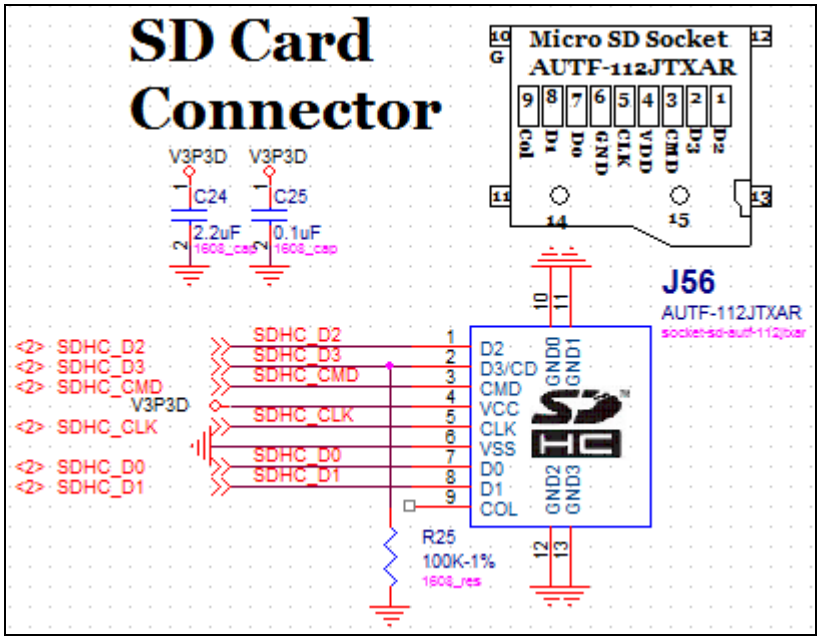
2-10 RTC

RTC는 R20023T-TE로 TWI로 I/F 되어 있고 alarm 기능이 내장 되어있다.



2-11 SD Card

SD Card는 micro sd card로 HC mode를 지원한다.



2-12 Power

AMAZONES-BASE는 5V~12V의 전원을 사용 할 수 있다.

2-13 Board to Board Connect(CON1, CON2)

Connector 사용시 multiplexed pin에 주의 해야 한다. 또한 아래의 pin들은 사용 시 주의 해야 한다.

*CON1의 35,37,38,39,40은 boot mode로 사용 되므로 출력전용으로 사용해야 한다.

*CON2의 49,50,51,52,53,54,55,56, 59,60,61,62,63,64는 NAND Flash에서 사용하므로 사용자는 이 pin을 사용할 수 없다.

■ CON1

CON1 Right Side					CON1 Left Side			
Pin No	1ST Name	2nd Name	3rd Name		Pin No	1ST Name	2nd Name	3rd Name
1	5.0V				2	5.0V		
3	5.0V				4	5.0V		
5	5.0V				6	5.0V		
7	5.0V				8	5.0V		
9	NC				10	NC		
11	GND				12	GND		
13	GND				14	GND		
15	Y/G				16	GND		
17	GND				18	GND		
19	Pb?B				20	GND		
21	GND				22	GND		
23	Pr/R/CVBS				24	GND		
25	GND				26	GP14_7		
27	GP14_4				28	GP14_6		
29	GP14_2				30	GP14_5		
31	GP14_0				32	GP14_3		
33	SRAM_nWAIT		GP11_6		34	GP14_1		
35	SRAM_A20	BOOT4	GP11_4		36	SRAM_A21	LCD_VCLKIN	GP11_5
37	SRAM_A18	BOOT2	GP11_2		38	SRAM_A19	BOOT3	GP11_3
39	SRAM_A16	BOOT0	GP11_0		40	SRAM_A17	BOOT1	GP11_1
41	SRAM_D14	SPI_MISO1	GP10_6		42	SRAM_D15	SPI_MOSI1	GP10_7
43	SRAM_D12	SPI_nCS1	GP10_4		44	SRAM_D13	SPI_SCK1	GP10_5
45	SRAM_D10	PWMOUT2	GP10_2		46	SRAM_D11	CAN_IN2	GP10_3
47	SRAM_D8	UART_TX2	GP10_0		48	SRAM_D9	UART_RX2	GP10_1

49	SRAM_D6		GP9_6	50	SRAM_D7		GP9_7
51	SRAM_D4		GP9_4	52	SRAM_D5		GP9_5
53	SRAM_D2		GP9_2	54	SRAM_D3		GP9_3
55	SRAM_D0		GP9_0	56	SRAM_D1		GP9_1
57	SRAM_A14	I2S_RX_WS1	GP8_6	58	SRAM_A15	EIRQ1	GP8_7
59	SRAM_A12	I2S_SDI1	GP8_4	60	SRAM_A13	I2S_RX_SCLK1	GP8_5
61	SRAM_A10	I2S_TX_WS1	GP8_2	62	SRAM_A11	I2S_SDO1	GP8_3
63	SRAM_A8	I2S_CDCLK1	GP8_0	64	SRAM_A9	I2S_TX_SCLK1	GP8_1
65	SRAM_A6		GP7_6	66	SRAM_A7		GP7_7
67	SRAM_A4		GP7_4	68	SRAM_A5		GP7_5
69	SRAM_A2		GP7_2	70	SRAM_A3		GP7_3
71	SRAM_A0		GP7_0	72	SRAM_A1		GP7_1
73	ICE_VDIN6	I2S_RX_WS1	GP4_6	74	ICE_VDIN7	ERIQ0	GP4_7
75	ICE_VDIN4	I2S_SDI1	GP4_4	76	ICE_VDIN5	I2S_RX_SCLK1	GP4_5
77	ICE_VDIN2	I2S_TX_WS1	GP4_2	78	ICE_VDIN3	I2S_SDO1	GP4_3
79	ICE_VDIN0	I2S_CDCLK1	GP4_0	80	ICE_VDIN1	I2S_TX_SCLK1	GP4_1
81	SF_nCS		GP5_6	82	SF_CLK		GP5_7
83	TWI_SCL		GP5_4	84	TWI_SDA		GP5_5
85	SPI_MISO0	PWM_OUT3	GP5_2	86	SPI_MOSI0	CANP_IN3	GP5_3
87	SPI_nCS0	UART_TX3	GP5_0	88	SPI_SCK0	UART_RX3	GP5_1
89	SRAM_nBE1		GP6_6	90	SRAM_nCS0		GP6_7
91	SRAM_nWE		GP6_4	92	SRAM_nRE		GP6_5
93	SF_D2		GP6_2	94	SF_D3		GP6_3
95	SF_D0		GP6_0	96	SPI_D1		GP6_1
97	GND			98	GND		
99	GND			100	GND		

표 2-1 CON1

■ CON2

CON2 Right Side				CON2 Left Side			
Pin No	1ST Name	2nd Name	3rd Name	Pin No	1ST Name	2nd Name	3rd Name
1	SND_I2S_MCLK			2	SND_I2S_SCLK		
3	SND_I2S_LRCLK			4	5SND_I2S_SDO		

5	SND_I2S_SDI			6	CAP_IN1	SRAM_nCS3	GP12_3
7	GND			8	PWOM_OUT1	SRAM_nCS2	GP12_2
9	LCD_VSYNC			10	UART_RX1	USB_HOST_CUR	GP12_1
11	GND			12	UART_TX1	USB_HOST_POW	GP12_0
13	EIRQ0	LCD_VCLKOUT	GP11_7	14	LCD_HSYNC		
15	GND			16	LCD_DISPEN		
17	LCD_R0			18	LCD_R1		
19	LCD_R2			20	LCD_R3		
21	LCD_R4			22	LCD_R5		
23	LCD_R6			24	LCD_R7		
25	LCD_G0			26	LCD_G1		
27	LCD_G2			28	LCD_G3		
29	LCD_G4			30	LCD_G5		
31	LCD_G6			32	LCD_G7		
33	LCD_B1			34	LCD_B1		
35	LCD_B3			36	LCD_B3		
37	LCD_B5			38	LCD_B5		
39	LCD_B7			40	LCD_B7		
41	GP13_6			42	GP13_7		
43	GP13_4			44	GP13_5		
45	GP13_2			46	GP13_3		
47	GP13_0			48	GP13_1		
49	NF_D6	PWM_OUT2	GP0_6	50	NF_D7	CAP_IN2	GP0_7
51	NF_D4	UART_TX2	GP0_4	52	NF_D5	UART_RX2	GP0_5
53	NF_D2	PWM_OUT1	GP0_2	54	NF_D3	CAP_IN1	GP0_3
55	NF_D0	UART_TX1	GP0_0	56	NF_D1	UART_RX1	GP0_1
57	UART_TX0		GP1_6	58	UART_RX0		GP1_7
59	NF_nRE		GP1_4	60	NF_nBUSY		GP1_5
61	NF_CLE		GP1_2	62	NF_nWE		GP1_3
63	NF_nCS		GP1_0	64	NF_ALE		GP1_1
65	GND			66	GND		
67	USB_DP			68	GND		
69	USB_DM			70	nRESET		
71	GND			72	GND		
73	JTAG_TCK			74	JTAG_TDI		

75	GND			76	JTAG_TMS		
77	JTAG_TDO			78	JTAG_TRST		
79	GND			80	GND		
81	PWM_OUT0		GP2_6	82	CAP_IN0	SRAM_nCS1	GP2_7
83	SDHC_CLK		GP2_4	84	SDHC_CMD		GP2_5
85	SDHC_D2	PWM_OUT3	GP2_2	86	SDHC_D3	CANPIN3	GP2_3
87	SDHC_D0	UART_TX3	GP2_0	88	SDHC_D1	UART_RX3	GP2_1
89	I2S_RX_WS0		GP3_6	90	ICE_VCLK		GP3_7
91	I2S_SDI0		GP3_4	92	I2S_RX_SCLK0		GP3_5
93	I2S_TX_WS0		GP3_2	94	I2S_SDO0		GP3_3
95	I2S_CDCLK0		GP3_0	96	I2S_TX_SCLK0		GP3_1
97	GND			98	GND		
99	GND			100	GND		

丞 2-2 CON2